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(71) Applicant: MOTOROLA INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: BIERACH, Kirk, Bradley; 20355 Orchard Road, Saratoga, CA 95070 (US). LOVING, Sean, Thomas; 2040 W. Middlefield Road #8, Mountain View, CA 94043 (US). FITZPATRICK, Mark, Daniel; 1497 Cabrillo Avenue, Santa Clara, CA 95050 (US).

(74) Agents: EGAN, Wayne, J. et al.; Motorola Inc., Intellectual Property Dept., 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

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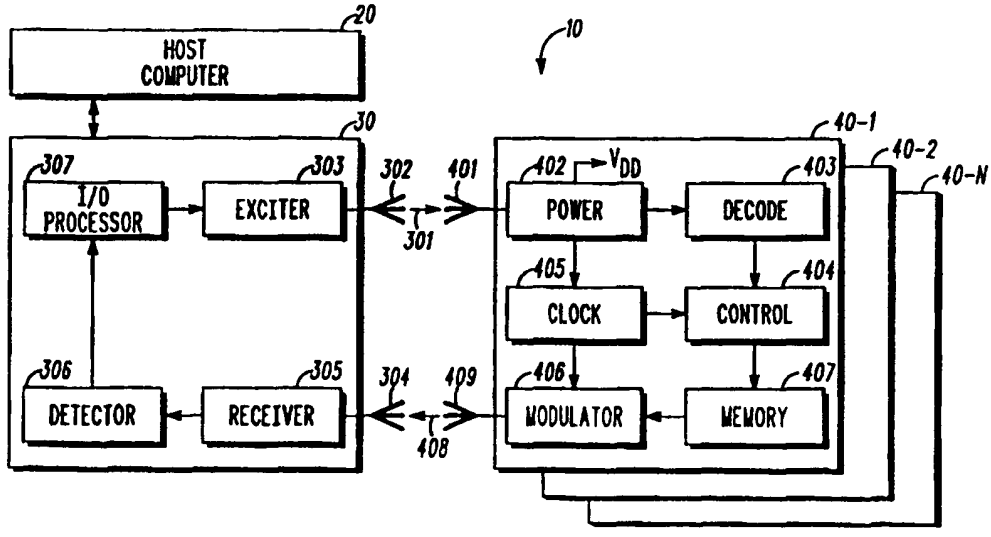

(57) Abstract

A synchronization method for an RFID system (10) including tags (40–1 to 40–n) having different memory sizes, employs a convention wherein sync words and sync bits are stored in tag memory (407) among data bits so that a reader (30) may readily identify the sync word on an RF signal (408) transmitted by a tag (40–1) and serially modulated by repetitions of the contents of the tag memory (407). After identifying the sync word, an RFID reader (30) reads data bits following the identified sync word until a next sync word is received, while ignoring the sync bits interspersed among the data bits.

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SYNCHRONIZATION METHOD FOR RFID SYSTEM INCLUDING TAGS HAVING DIFFERENT MEMORY SIZES

Reference to Prior Provisional Application

The applicant hereby claims the priority benefit of prior provisional application number 60/077,987 filed 13 March 1998 by Kirk B. Bierach et al., the same inventors as in the present application, and the disclosure of which prior provisional application is hereby incorporated by reference verbatim, with the same effect as though such disclosure were fully and completely set forth herein.

Field of the Invention

This invention relates generally to RFID systems and in particular, to RFID systems including tags having different memory sizes.

Background of the Invention

Radio frequency identification (RFID) systems are well known, and find numerous uses. For example, RFID systems are used in access control applications where employees use RFID "proximity" cards or tags to gain access to authorized areas, or tags are bolted to the undercarriage of transport trucks and other types of vehicles to allow them access to a facility. As another example, RFID systems are used in animal identification applications where individualized tags are placed on the ears of livestock to identify each animal. In yet another example, RFID systems are used in container tracking applications where individualized

tags are fixed to reusable containers to facilitate accurate records of their use.

In these and other applications, RFID tags (also referred to as "transponders" or "labels") typically transmit multiple blocks of data to RFID readers. The number and size of the data blocks transmitted may be different among tags, however, due to differences in application requirements or differences in the memory structures storing such data within the tags. Differences in memory or data structures result from different numbers of data blocks or different numbers of bits in each data block being transmitted. Different manufacturers of the tags or the memories employed in the tags are one cause for the different memory structures being used in the tags. Advancements in manufacturing techniques are another cause.

In conventional RFID systems, however, data are generally communicated in fixed quantities as defined by the particular system since such systems lack capability to read tags transmitting data blocks of arbitrary size or number. Such systems are therefore constrained to be incompatible among existing and future commercially available tag offerings, and their resulting intersystem inoperability tends to increase the overall cost of using such systems. Industry standardization would help to eliminate such problems.

Thus, there is a need for a "Synchronization Method for RFID System Including Tags Having Different Memory Sizes".

Summary of the Invention

It is one object of the present invention to provide an RFID system capable of reading data transmitted from tags having different memory sizes, resulting from variable size and number of data blocks among the tags.

Another object is to provide synchronization method and means to facilitate the transmission and reading of data from RFID tags having different memory sizes.

These and additional objects are accomplished by the various aspects of the present invention, wherein, briefly stated, one aspect of the invention is a synchronization method for an RFID system including tags having different memory sizes, comprising the steps of: storing a sync word in a first area in a tag memory, and storing data bits and sync bits in a second area in the tag memory such that the sync word cannot occur in the data bits and the sync bits.

In another aspect, a synchronization method for an RFID system including tags having different memory sizes, comprises the steps of: transmitting a sync word serially modulated on an RF signal, and transmitting data bits and sync bits serially modulated on the RF signal such that the sync word cannot occur in the data bits and the sync bits.

In another aspect, a synchronization method for an RFID system including tags having different memory sizes, comprises the steps of: receiving an RF signal serially modulated by repetitions of contents of a tag memory storing a sync word, data bits, and sync bits such that the sync word cannot occur within the data bits and the sync bits; identifying one of the repetitions of the sync word serially modulated on the RF signal; and reading data bits following the one of the repetitions of the sync word serially modulated on the RF signal, until a next one of the repetitions of the sync word is received serially modulated on the RF signal.

In yet another aspect, an RFID tag for an RFID system including tags having different memory sizes, comprises a tag memory, a control circuit and a modulator circuit. The tag memory has a sync word stored at one end of the tag memory, and data bits and sync bits stored in a remainder of the tag memory such that the sync word cannot occur in the

remainder of the tag memory. The control circuit provides address and control signals to the tag memory so as to read out contents of the tag memory. The modulator circuit generates an RF signal serially modulated by the contents of the tag memory.

In still another aspect, an RFID reader for an RFID system including tags having different memory sizes, comprises a receiver circuit and a processor. The receiver circuit is coupled to an RF signal serially modulated by repetitions of a sync word, data bits, and sync bits organized such that the sync word cannot occur within the data bits and the sync bits. The processor is coupled to the receiver circuit. The processor includes a memory storing a program causing the processor to identify one of the repetitions of the sync word, and to read data bits following the one of the repetitions of the sync word until a next one of the repetitions of the sync word is received.

In yet one more aspect, an RFID system including tags having different memory sizes, comprises a plurality of tags and an RFID reader. The plurality of tags individually include a tag memory, a control circuit and a modulator circuit. The tag memory has a sync word stored at one end of the tag memory and data bits and sync bits stored in a remainder of the tag memory such that the sync word cannot occur in the data bits and the sync bits. The control circuit provides address and control signals to the tag memory so as to read out contents of the tag memory. The modulator circuit generate an RF signal serially modulated by repetitions of the contents of the tag memory. The RFID reader, on the other hand, includes a receiver circuit and a processor. The receiver circuit is coupled to the RF signal, and the processor. The processor includes a memory storing a program causing the processor to identify one of the repetitions of the sync word serially modulated on the RF signal, and to read data bits following the one of the repetitions of the sync word until a next one of the repetitions of the sync word is received on the

Additional objects, features and advantages of the various aspects of the present invention will be apparent from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a block diagram of an RFID system including tags having different sizes, utilizing aspects of the present invention.

FIG. 2 is an example of a tag memory organization including a 32-bit sync word, utilizing aspects of the present invention.

FIG. 3 is an example of a tag memory organization including a 24-bit sync word, utilizing aspects of the present invention.

FIG. 4 is an example of a tag memory organization including a 16-bit sync word, utilizing aspects of the present invention.

FIG. 5 is an example of a tag memory organization including a 9-bit sync word, utilizing aspects of the present invention.

FIG. 6 is an example of a tag memory organization including a 16-bit sync word beginning at a beginning address of the tag memory, utilizing aspects of the present invention.

FIG. 7 is an example of a tag memory organization including a 16-bit sync word ending at an ending address of the tag memory, utilizing aspects of the present invention.

FIG. 8 is a first example of a prior art tag memory organization.

FIG. 9 is a second example of a prior art tag memory organization.

FIG. 10 is a third example of a prior art tag memory organization.

FIG. 11 is an example of repetitions of the contents of any one of the first, second, or third examples of a prior art tag memory organization.

FIG. 12 is a flow diagram of a synchronization method for an RFID system including tags having different memory sizes, utilizing aspects of the present invention.

Description of the Preferred Embodiments

FIG. 1 is a block diagram of an RFID system 10 including tags having different memory sizes. Included in the RFID system 10 are a host computer 20, an RFID reader 30, and a plurality of RFID tags 40-1 to 40-n having different memory sizes. RFID tag 40-1 is representative of the RFID tags 40-1 to 40-n, and for the purposes of the following discussion, RFID tag 40-1 is assumed to be proximate to the RFID reader 30 so that its one or more antenna elements 401 receive an exciter signal 301 transmitted through corresponding one or more antenna elements 302 of the RFID reader 30. An exciter circuit 303 of the RFID reader 30 generates the exciter signal 301.

A power circuit 402 on the RFID tag 40-1 rectifies the received exciter signal 301 to generate an internal supply voltage Vdd for other circuitry on the RFID tag 40-1. If commands or data are superimposed or modulated onto to a carrier signal of the exciter signal 301, the power circuit 402 passes the exciter signal 301 to a decode circuit 403. The decode circuit 403 demodulates the exciter signal 301 and performs an analog-to-digital conversion to produce the command or data in digital form, which it provides to a control circuit 404. The power circuit 402 also passes the exciter signal 301 to a clock generator circuit 405.

The clock generator circuit 405 generates two clock signals. One clock signal has the same frequency as the exciter carrier signal, and is provided to the control circuit 404. The other clock signal has a different frequency than the exciter carrier signal, and is provided to a modulator circuit 406 to serve as a tag carrier signal for an RF signal 408 transmitted from the RFID tag 40-1. In the preferred embodiment, the frequency of the tag carrier signal is approximately half that of the exciter carrier signal to distinguish the two carrier signals.

The control circuit 404 includes an address counter (not shown) which increments the address to a tag memory 407. In response to the exciter signal 301, the control circuit 404 generates appropriate control signals to cause information to be repetitively read out of the tag memory 407 in a serial fashion at the rate of the exciter carrier signal. The information is then provided to the modulator circuit 406. The modulator circuit 406 superimposes or modulates the information onto the tag carrier signal to generate the RF signal 408 serially modulated by repetitions of the contents of the tag memory 407. In the preferred embodiment, the RF signal 408 is serially modulated by repetitions of a sync word, data bits, and sync bits oganized such that the sync word cannot occur within the data bits and the sync bits. A transmitting antenna 409 coupled to the modulator circuit 406 transmits the RF signal 408 to a receiving antenna 304 on the RFID reader 30.

A receiver circuit 305 is coupled to the RF signal 408 through the receiving antenna 304, to receive and amplify the RF signal 408. The receiver circuit 305 preferably also converts the frequency of the RF signal 408 to an intermediate frequency for further amplification and bandpass filtering before providing it to a detector circuit 306. The detector circuit 306 detects information serially modulated on the RF signal 408, and provides the information to a processor 307, which produces an output in a format usable by the host computer 20. The processor 307 includes a memory (not shown) storing a program to be executed by the processor 307. The host computer 20 processes the information passed to it by the processor 307.

The tag memory 407 may be different sizes by being configured in various memory or data structures having different numbers of blocks and/or different numbers of bits per block. For example, FIG. 2 illustrates a data structure for tag memory 407 having 7 blocks of 32 bits each, FIG. 6 illustrates a data structure having 7 blocks of 16 bits each, and FIG. 8

illustrates a data structure having 3 blocks of 5 hexadecimal characters each (or 20 bits each, since each hexadecimal character is 4 bits).

Since the contents of the tag memory 407 are read out repetitively to be serially modulated on the RF signal 408, it may be difficult or impossible for the RFID reader 30 to determine the repetitive pattern (i.e., contents of the tag memory 407) without prior knowledge of the data structure. For example, in FIG. 8, the pattern "0123456789ABCDE" is stored in a first example of a prior art tag memory organization; in FIG. 9, the pattern "56789ABCDE01234" is stored in a second example of a prior art tag memory organization; and in FIG. 10, the pattern "ABCDE0123456789" is stored in a third example of a prior art tag memory organization. Yet problematically, each of these patterns generate the same repetitive or recursive pattern depicted in FIG. 11, as information is read out of the tag memory 407 starting in the top left corner, reading to the right along each block, reading blocks from top to bottom, and ending in the bottom right corner. As another example, in certain repetitive patterns such as all 1's, all 0's, or alternating 1's and 0's, it is also virtually impossible for the RFID reader 30 to determine the length of the recurring pattern without prior knowledge of the data structure.

Accordingly, it is an aspect of the present invention to include a sync word beginning at the beginning address of the tag memory 407, or ending at the ending address of the tag memory 407, so that the RFID reader 30 can properly read the contents of the tag memory 407 from the RF signal 408. To ensure that the sync word is not inadvertently replicated somewhere else in the recurring pattern, sync bits are interspersed at appropriate bit locations in the recurring pattern. The RFID reader 30 may then determine the recurring pattern by first finding the sync word, then reading the data following the sync word until a next

occurrence of the sync word, while ignoring, masking or stripping off the sync bits.

Referring briefly to FIG. 6, a sync word 52 is shown as "1000000000000001" beginning at a beginning address of the tag memory 407, sets of sync bits of "01" such as the set of sync bits 54 in the seventh block of the memory structure are interspersed among data bits "x" such as data bits 56 such that the sync word cannot occur within the data bits and sync bits. The sync word and sync bits are also referred to as "system bits", and the data bits as "user data bits". Successive data bits between the sync word and a set of sync bits, or between sets of sync bits, are referred to as "data words" such as data word 58 in the second block of the tag memory 407. FIG. 7 illustrates another example of a data structure where the sync word ends at the ending address of the tag memory 407.

In order to readily identify the sync word, the sync word is predefined as a bit pattern in which the largest number of 0's are sandwiched between two 1's within the contents of the data structure. To ensure that the sync word includes the largest number of 0's sandwiched between two 1's, sets of sync bits of "01" are periodically inserted among the data bits such that the number of data bits between adjacent sets of sync bits is less than or equal to four (4) bits less than the number of bits in the sync word. Alternatively, a single sync bit of "1" may be used instead of the pair of sync bits "01". In this case, the number of data bits between adjacent sync bits would be less than or equal to three (3) bits less than the number of bits in the sync word.

Although the number of data bits between adjacent sets of sync bits "01" may be less than four bits less than the number of bits in the sync word, preferably the number of data bits between adjacent sets of sync bits is set equal to four bits less than the number of bits in the sync word so that the maximum number of bits are made available in the data

structure for data bits. Also, by following this convention, the locations of the sync bits are thus readily determinable after the RFID reader 30 has identified the sync word, making it easier for the RFID reader 30 to mask out or strip off the sync bits while reading the data bits serially modulated on the RF signal 408.

Further, by following a convention where the sync word includes the entire first data block, such as depicted in FIG. 2, the data structure of the tag memory 407 is also readily determinable by the RFID reader 30. This convention, however, may not be practical for data structures including a relatively small number of blocks. Further, a shorter sync word such as shown in FIG. 3 sometimes allows more data bits to be available in the tag memory 407 than a sync word using up the entire first block. However, as shown in FIG. 4 and FIG. 5, this is not generally the case.

Thus, in summary, by storing sync words and sync bits of a known convention in the memory 407, the RFID reader 30 may readily determine the contents or repetitive pattern stored therein from information modulated on a received RF signal 408. Implementation of the RFID reader 30 is straightforward, and within the skill of one of ordinary skill in the art.

FIG. 12 illustrates a flow diagram of a synchronization method for the RFID system 10 including tags 40-1 to 40-n having different memory sizes. A first step 1201 comprises the step of storing a sync word in a first area in a tag memory. The first area is preferably successive bit locations beginning at a beginning address of the tag memory such as depicted in FIG. 6. In this case, the step of storing a sync word, comprises the step of storing a sync word in successive bit locations beginning at a beginning address of said tag memory. Alternatively, the first area may be successive bit locations ending at an ending address of the tag memory such as depicted in FIG. 7. In such case, the step of storing a sync word, comprises the step of storing a sync word in successive bit locations

ending at an ending address of said tag memory. Since the sync word is predefined preferably as a bit pattern in which the largest number of 0's are sandwiched between two 1's within the contents of the data structure of the tag memory, the step of storing a sync word, comprises the steps of: storing one bit of a first binary state, storing a plurality of bits of a second binary state, and storing one bit of said first binary state. The storing of the sync word is preferably performed by programming the tag memory by conventional methods and means after manufacture. However, the storing of the sync word can be alternatively performed with similar benefit during the manufacturing process of the tag memory or the tag by conventional methods and means.

A second step 1202 comprises the step of storing data bits and sync bits in a second area in said tag memory such that said sync word cannot occur in said data bits and said sync bits. The second area is a remainder of the tag memory after storing the sync word in the tag memory. In general terms, the sync bits are interspersed among said data bits such that said sync word cannot occur in said remainder of said tag memory. More particularly, the step of storing data bits and sync bits, comprises the steps of: organizing data bits into data words individually having a number of data bits at least four less than a number of bits in said sync word; organizing sync bits into sets of sync bits individually having at least one bit of said first binary state; and storing said data words and said sets of sync bits in said tag memory by interleaving said sets of sync bits with said data words. The storing of the data bits and sync bits is preferably performed by programming the tag memory by conventional methods and means after manufacture. However, the storing of the data bits and sync bits can be alternatively performed with similar benefit during the manufacturing process of the tag memory or the tag by conventional methods and means.

A third step 1203 comprises the step of transmitting a sync word serially modulated on an RF signal. Preferably, said step of transmitting said sync word, comprises the steps of: transmitting one bit of a first binary state; transmitting a plurality of bits of a second binary state; and transmitting one bit of said first binary state. To perform such step, the control circuit 404 in the tag memory 407 generates appropriate control signals to cause information to be repetitively read out of the tag memory 407 in a serial fashion, and provided to the modulator circuit 406 which generates an RF signal 408 serially modulated by contents of the tag memory 407. A transmitting antenna 409 coupled to the modulator circuit 406 thereupon transmits the RF signal 408.

A fourth step 1204 comprises the step of transmitting data bits and sync bits serially modulated on said RF signal such that said sync word cannot occur in said data bits and said sync bits. Preferably, said step of transmitting data bits and sync bits, comprises the step of transmitting data bits organized into data words individually having a number of data bits at least four less than a number of bits in said sync bit, and sync bits organized into sets of sync bits individually having at least one bit of said first binary state, such that said sets of sync bits are interleaved with said data words. To perform such step, the control circuit 404 in the tag memory 407 generates appropriate control signals to cause information to be repetitively read out of the tag memory 407 in a serial fashion, and provided to the modulator circuit 406 which generates an RF signal 408 serially modulated by contents of the tag memory 407. A transmitting antenna 409 coupled to the modulator circuit 406 thereupon transmits the RF signal 408.

A fifth step 1205 comprises the step of receiving an RF signal serially modulated by repetitions of contents of a tag memory storing a sync word, data bits, and sync bits such that said sync word cannot occur within said data bits and said sync bits. To perform such step, the

receiver 305 is coupled to the receiving antenna 304, to receive and amplify the RF signal 408, as described in reference to FIG. 1.

A sixth step 1206 comprises the step of identifying one repetition of said sync word serially modulated on said RF signal. Preferably, the step of identifying one repetition of said sync word, comprises the step of finding a longest sequence of bits of said second binary state serially modulated on said RF signal. Since the sync word is organized as one bit of a first binary state, a plurality of bits of a second binary state, and one bit of said first binary state, this entails finding the longest sequence of bits of the second binary state serially modulated on the RF signal. To perform such step, the processor 307 includes a memory (not shown) storing a program which causes the processor 307 to identify one repetition of said sync word by finding a maximum number of consecutive bits in the second binary state, using conventional programming methods.

A seventh step 1207 comprises the step of reading data bits following said one of said repetitions of said sync word serially modulated on said RF signal, until a next repetition of said sync word is received serially modulated on said RF signal. Preferably, said step of reading data bits comprises the steps of: (a) reading a number of successive data bits, said number being four bits less than the number of bits of said sync word; (b) reading a next bit following said number of successive data bits; and (c) if said next bit is in said first binary state, then stopping, or, if said next bit is in said second binary state, then ignoring a bit following said next bit and jumping back to step (a). To perform such steps, the processor 307 includes a memory (not shown) storing a program which causes the processor 307 to perform such steps, using conventional programming methods.

One advantage of the present invention is an RFID system capable of reading data transmitted from tags having different memory sizes, allowing compatibility among existing and future commercially available

tag offerings. Another advantage is an RFID system capable of reading data transmitted from tags having different memory sizes, allowing intersystem operability and reduction in the overall cost of such system.

While particular embodiments of the invention have been described in detail herein, it will be appreciated that various modifications can be made to the preferred embodiment without departing from the scope of the invention. Thus, the foregoing description is not intended to limit the invention which is defined in the appended claims.

Claims:

1. An RFID tag for an RFID system including tags having different memory sizes, comprising:

a tag memory having a sync word stored at one end of said tag memory, and data bits and sync bits stored in a remainder of said tag memory such that said sync word cannot occur in said remainder of said tag memory,

a control circuit providing address and control signals to said tag memory so as to read out contents of said tag memory, and

a modulator circuit generating an RF signal serially modulated by said contents of said tag memory.

2. The RFID tag according to claim 1, wherein said sync word comprises one bit of a first binary state, a plurality of bits of a second binary state, and one bit of said first binary state.

3. The RFID tag according to claim 2, wherein said sync bits are interspersed among said data bits such that said sync word cannot occur in said remainder of said tag memory.

4. The RFID tag according to claim 3, wherein said data bits are organized into data words individually having a number of data bits which is four bits less than a number of bits of said sync word, said sync bits are organized into sets of sync bits including at least one bit of said first binary state, and said sets of sync bits are interleaved with said data words.

5. An RFID reader for an RFID system including tags having different memory sizes, comprising:

a receiver circuit coupled to an RF signal serially modulated by repetitions of a sync word, data bits, and sync bits organized such that said sync word cannot occur within said data bits and said sync bits, and

a processor coupled to said receiver circuit, said processor including a memory storing a program causing said processor to identify

one repetition of said sync word, and to read data bits following said one repetition of said sync word until a next repetition of said sync word is received.

6. The RFID reader according to claim 5, wherein each of said sync words comprises one bit of a first binary state, a plurality of bits of a second binary state, and one bit of said first binary state.

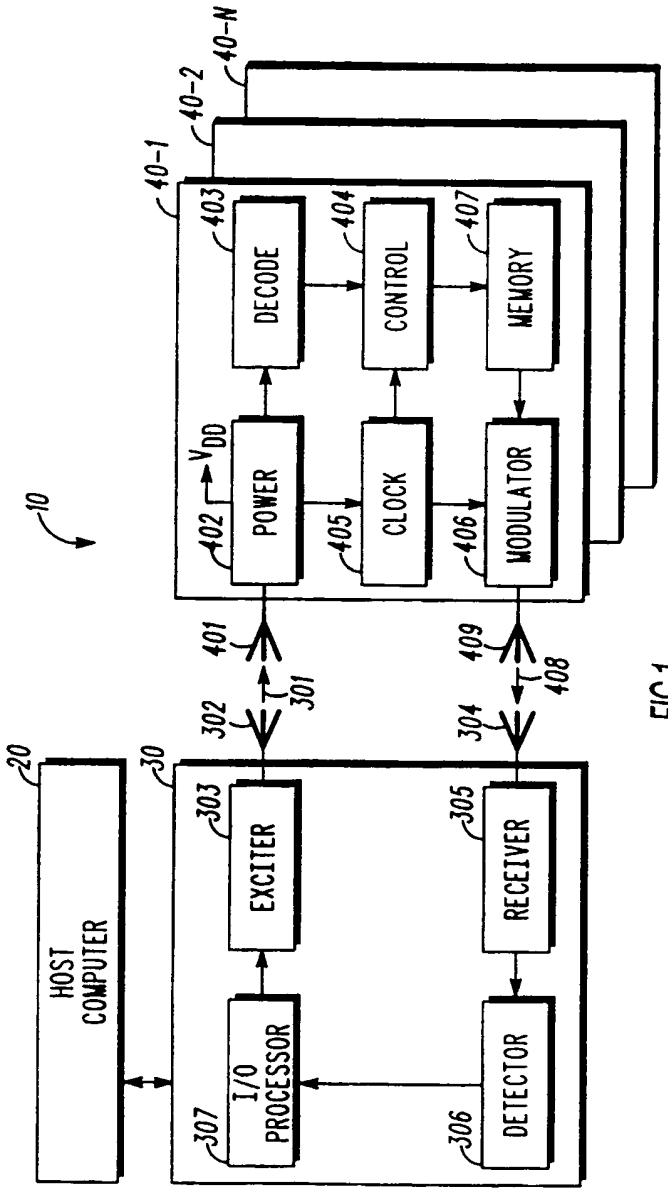
7. The RFID reader according to claim 6, wherein said data bits are organized into data words individually having a number of data bits which is four bits less than a number of bits of said sync word, said sync bits are organized into sets of sync bits including at least one bit of said first binary state, and said sets of sync bits are interleaved with said data words.

8. The RFID reader according to claim 7, wherein said program causes said processor to identify one repetition of said sync word by finding a longest sequence of bits of said second binary state.

9. An RFID system including tags having different memory sizes, comprising:

a plurality of tags individually including a tag memory, a control circuit and a modulator circuit, said tag memory having a sync word stored at one end of said tag memory and data bits and sync bits stored in a remainder of said tag memory such that said sync word cannot occur in said data bits and said sync bits, said control circuit providing address and control signals to said tag memory so as to read out contents of said tag memory, and said modulator circuit generating an RF signal serially modulated by repetitions of said contents of said tag memory, and

an RFID reader including a receiver circuit and a processor, said receiver circuit coupled to said RF signal, and said processor including a memory storing a program causing said processor to identify one repetition of said sync word serially modulated on said RF signal, and to read data bits following said one repetition of said sync word until a next repetition of said sync word is received on said RF signal.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408
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EXCITER
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I/O PROCESSOR
306
DETECTOR

FIG.1

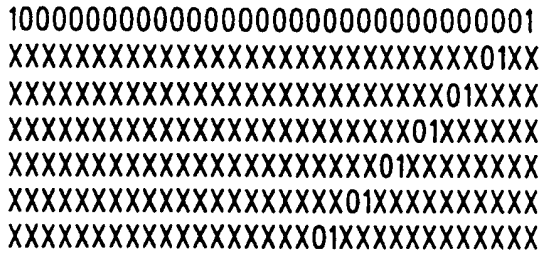

FIG.2

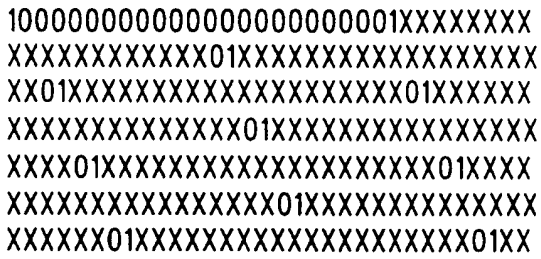

FIG.3

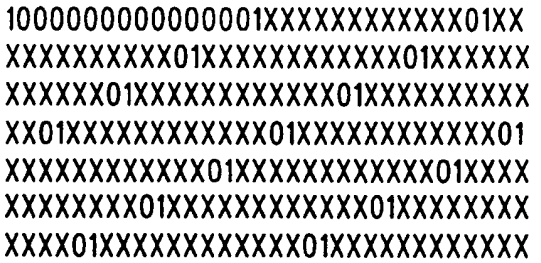

FIG.4

FIG.5

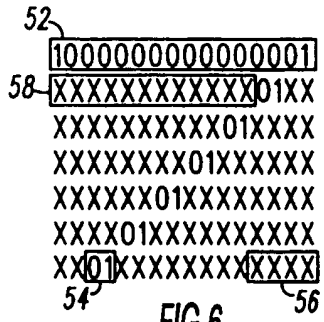

FIG.6

XXXXXXXXXXXX01XX
XXXXXXXXXX01XXXX
XXXXXXXX01XXXXXX
XXXXXX01XXXXXXXX
XX01XXXXXXXXXXXX
1000000000000001

FIG.7

01234
56789
ABCDE

FIG.8
—PRIOR ART—

56789
ABCDE
01234

FIG.9
—PRIOR ART—

ABCDE
01234
56789

FIG.10
—PRIOR ART—

...0123456789ABCDE0123456789ABCDE...

FIG.11
—PRIOR ART—

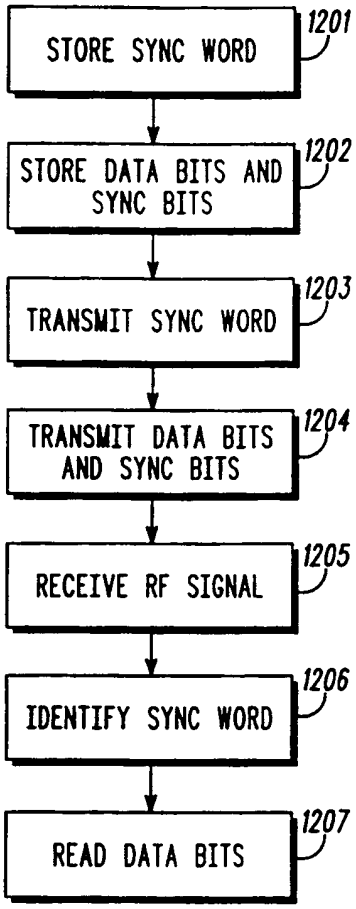
STORE SYNC WORD
1201
STORE DATA BITS AND SYNC BITS
1202
TRANSMIT SYNC WORD
1203
TRANSMIT DATA BITS AND SYNC BITS
1204
RECEIVE RF SIGNAL
1205
IDENTIFY SYNC WORD
1206
READ DATA BITS
1207

FIG.12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/04860

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04Q 1/00; G06F 17/00; G08G 1/01; G06F 11/10
US CL : 235/491, 375, 492, 379; 340/825.54, 572, 928,
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 235/491, 375, 492, 379; 340/825.54, 572, 928,

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

U.S. PTO APS
search terms: s RFID (10a) reader? and tag? and memory? and sync?

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US 5,818,348 A (WALCZAK ET AL) 06 OCTOBER 1998 (06/10/98), see entire document	1-9
Y	US 5,621,199 A (CALARI ET AL) 15 April 1997 (15/04/97). see entire document	1-9
Y,P	US 5,805,082 A (HASSET) 08 September 1998 (08/09/98), see entire document	1-9
Y	US 4,888.773 (ARLINGTON ET AL) 19 DECEMBER 1989 (19/12/89), see entire document	1-9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 11 MAY 1999	Date of mailing of the international search report 26 MAY 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer DANIEL FELTEN Telephone No. (703) 308-0724

Form PCT/ISA/210 (second sheet)(July 1992)*